UNITED STATES PATENT AND TRADEMARK OFFICE

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09/872,962	06/01/2001	James M. Reuter	P01-3663	4878

22879 7590 01/26/2007 HEWLETT·PACKARD COMPANY P O BOX 272400, 3404 E. HARMONY ROAD INTELLECTUAL PROPERTY ADMINISTRATION FORT COLLINS, CO 80527-2400	**EXAMINER** NAWAZ, ASAD M

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Application Number: 09/872,962
Filing Date: June 01, 2001
Appellant(s): REUTER ET AL.

MAILED

JAN 26 2007

Technology Center 2100

Hewlett-Packard Development Company
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 11/03/06 appealing from the Office action

mailed 2/8/06.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

| 5,940,850 | Harish | 8-1999 |
| 5,483,649 | Kuznetzov | 1-1996 |

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Harish

et al (USPN 5940850) hereinafter referred to as Harish.

As to claim 1, Harish teaches a virtual storage system for mapping virtual storage

segments of differing sizes to storage locations, comprising:

an agent (Fig 1, 102) coupled to a host (fig 1, 100), the agent having volatile

memory (fig 1, 106) for storing a first table, (abstract; col 2, lines 25-34; col 3, lines 5-27;

RAM memory stores page table entries) the table having entries to map the virtual

storage segments to the storage locations; (Abstract; col 2, lines 25-34; col 4, lines 37-

50; page table entries in both RAM and ROM contain a mapping of virtual address to

physical address)

and a controller (fig 1, 108) coupled to the agent (fig 1, 102), the controller having

non-volatile memory (fig , 104) for storing a second table, (Abstract; col 2, lines 25-34;

col 4, lines 37-50; ROM memory stores page table entries) the controller intermittently

causing contents of the first table to be replaced by contents of the second table, (col 2,

lines 10-19; col 4, lines 43-50; the ROM data is loaded into RAM when memory is

modified)

whereby during an input/output (I/O) operation, the host accesses one of the

entries in the first table to determine one of the storage locations (Fig 2; col 2, lines 20-

34; the dynamic data as well as the page table entry is updated and a data page is also

allocated).

Claim 7 is essentially the system for claim 1, however it contains the following

additional limitations: a plurality of variables indicating states of the entry (Fig 3, col 4,

lines 20-37) and an offset for the entry, wherein the offset includes a logic unit number

identifier and a block identifier (col 2, lines 19-51 and col 3, lines 56 to col 4, line 5).

As to claim 2, Harish teaches the system of claim 1, wherein the second table

identifies an alternate storage location within the storage locations (col 3, lines 57-65

and col 4, lines 6-20).

As to claim 3, Harish teaches the system of claim 2, wherein the second table

further includes a bitmap having entries that correspond to blocks of data stored within

the alternate storage location (col 2, lines 20-34).

As to claim 4, Harish teaches the system of claim 1, further comprising an

alternate storage container comprising alternate storage locations of the storage

location correlating to the virtual storage segments (col 3, line 57 to col 4, line 5).

As to claim 5, Harish teaches the system of claim 4, wherein an I/O operation

accesses information on both the storage location and the alternative storage location

(col 4, lines 6-20).

As to claim 6, Harish teaches the system of claim 5 wherein a bitmap designates blocks at the alternative storage location to use for the I/O operation (col 3, line 57 to col 4, line 5).

As to claim 8, Harish teaches the system of claim 7, wherein said first memory is a volatile memory (abstract; col 2, lines 10-45; RAM memory).

As to claim 9, Harish teaches the system of claim 7, wherein said second memory is a non-volatile memory (abstract; col 2, lines 10-45; ROM memory).

As to claim 10, Harish teaches the system of claim 7, wherein the states include a no-write state (col 4, lines 6-20).

As to claim 11, Harish teaches the system of claim 7, wherein the states include an error state (abstract; col 4, lines 6-37).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 12-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harish et al (USPN 5,940,850) further in view of Kuznetzov (USPN 5,483,649).

As to claim 12, Harish et al teaches a method for performing an input/output operation on a virtual storage segment defined by a first table that maps the storage segment to a first storage location, the method comprising: identifying portions of the

virtual storage segment to be effected during the write operation; (col 2, lines 19-51 and col 3, lines 56-67).

storing a record of the identified portions at a second table and not at the first table (col 2, lines 19-51).

and writing to a second storage location, whereby the writing operation occurs at portions of the second storage location associated with the identified portions (col 2, lines 19-51 and col 3, lines 56-67).

However, Harish does not explicitly indicate turning off input/output operations at the first storage location.

Kuznetzov teaches turning off input/output operations at the first storage location (col 2, lines 14-30).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Kuznetzov into those of Harish in order to make the system more secure. Allowing various input/output operations to be enabled at the first storage location would make the system susceptible to numerous deficiencies, including system and/or data corruption.

As to claim 13, Kuznetzov teaches the method of claim 12, wherein the turning off step includes activating an invalid state (col 2, lines 14-30).

As to claim 14, Harish teaches the method of claim 12, wherein a subsequent read operation for the virtual segment occur at portions of the first storage location not included in the identified portions and the portions of the second storage location associated with the identified portions (col 2, lines 19-51 and col 3, lines 56-67).

As to claims 15, Harish teaches the method of claim 14, wherein the first table is stored by an agent and during the read operation, the record of the identified portions is sent to the agent (col 2, lines 19-51 and col 3, lines 56-67).

As to claim 16, Harish teaches the method of claim 15, wherein the mapping between the virtual storage segment and first storage location is contained in numerous first tables, each of the first table stored by a different agent (col 2, lines 19-51 and col 3, lines 56-67).

(10) Response to Argument

The examiner summarizes the various points raised by the appellant and addresses them individually.

At the onset, the examiner would like to point out that in the arguments section, appellant states that dependant claims 2, 3, 4, 5, 6, etc. are independent claims. The examiner respectfully disagrees and regards these statements as mere typographical errors. The claims are in dependent form and are thus treated as such.

As per appellant's arguments filed 11/3/06, the appellant argues:

Harish does not disclose or even suggest structural elements corresponding to

an agent, a host, and/or controller coupled to the agent as recited in claim 1 (see Brief,

page 8 -- Argument A).

In response to A), Harish discloses an agent (cpu) having a volatile memory.

The agent (cpu) is utilized for data collecting, calculation and control activities. The

processor is connected to a volatile memory (random access memory). The host

(overall computer system) includes the agent (cpu) and is thus coupled to the host.

Harish further discloses a controller (i/o controller) connected to the processor. The

controller is connected to non-volatile memory (ROM) and other devices providing input

to the controller (col 3, lines 6-27). Within each memory, ROM and RAM, is a page

table entry. If it is determined that the desired address is not in RAM during an i/o

operation, the page table within the ROM is loaded into the RAM replacing the existing

page table entry (col 4, lines 37-50).

Harish does not disclose or even suggest an arrangement in which the second

table identifies an alternate storage location within the storage locations (see Brief, page

11, -- Argument B).

In response to B) Harish teaches a second table identifying an alternate storage

location within the storage locations. Harish teaches the use of virtual addresses as

well as physical addresses. At any point in time, a number of pages are present in

memory which are tracked using a page table that cross references the virtual address

to the location of the actual page containing the memory data (col 3,lines 57-65).

Furthermore, the virtual memory manager creates a VMAP containing objects representing the data region of the system. The VMAP entries are remapped into the address space of each of the created tasks (col 4, lines 57-63).

Harish does not disclose the features of various claims (see Brief, page 13-20, -- Argument C).

In response to C), the examiner has twice rejected the presented claims in view of Harish (non-final rejection 10/11/05 and final rejection 2/8/06). The examiner has twice explained his position and presented a detailed mapping of the prior art to the claimed subject matter. However, the appellant generally argues various claims by simply stating a summary of the claim language followed by the examiner's cited portion. Thereafter, a general statement as to the prior art applied not disclosing the invention is presented. No explanation of why or how the prior art is defective is given. No specific contention of why the examiner's position is flawed or deficient is made. Therefore, the examiner directs attention to the explanation of the rejections applied in section 9, Grounds of Rejection above.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the

Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.
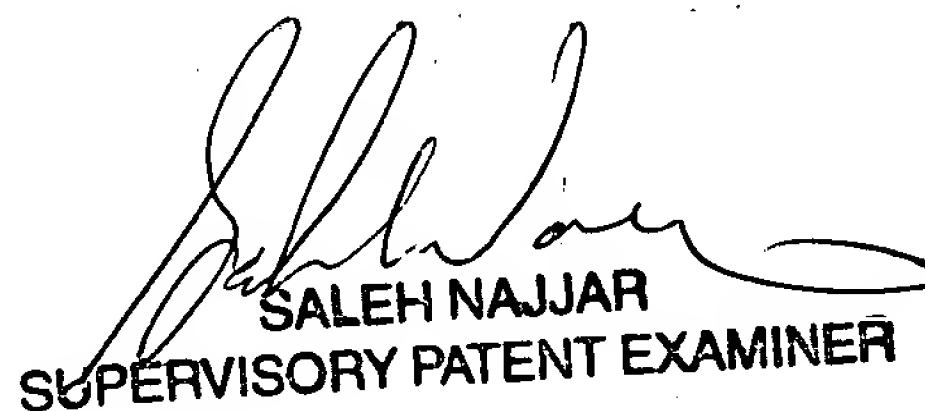
Respectfully submitted,

Asad M. Nawaz

January 18, 2006

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